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06EC63

Sixth Semester B.E. Degree Examination, December 2012
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With a neat diagram, explain the mixed signal layout strategy. **(07 Marks)**

b. Explain the different specifications of DAC. **(07 Marks)**

c. With a neat sketch, explain the typical errors associated with sample and hold circuit. **(06 Marks)**

2 a. With a neat diagram, explain the working of 3 bit pipeline DAC. **(07 Marks)**

b. With a neat circuit diagram, explain the working of R-2R ladder type DAC architecture. **(07 Marks)**

c. Determine the effective number of bits for a resistor string DAC which is assumed to be limited by the INL. The resistors are passive poly resistors with a known relative matching of 1% and V_{ref}= 5V. **(06 Marks)**

3 a. With the help of block diagram, explain the flash type ADC. **(07 Marks)**

b. With a neat block diagram, explain the working of successive approximation ADC. **(07 Marks)**

c. For an 8 bit single slope ADC with V_{ref} = 5V and clock frequency of 2 MHz, calculate the conversion time for an input of 2V. Also calculate the sampling frequency. **(06 Marks)**

4 a. With a neat block diagram, explain the working of voltage comparator. Also draw the schematic of pre-amplification stage of comparator. **(10 Marks)**

b. With a neat circuit diagram, explain the working of CMOS analog multiplier. Also explain the biasing of the multiplying quad. **(10 Marks)**

PART – B

5 a. With the help of block diagram explain the operation of an accumulate and dump circuit used for decimation and averaging. **(08 Marks)**

b. Explain the principle of interpolation and decimation. **(08 Marks)**

c. Determine the effective number of bits required for an ADC with a SNR of 50db. **(04 Marks)**

6 a. With neat sketches described the CMOS process. **(10 Marks)**

b. With neat CV curves explain natural MOSFET capacitor and floating MOS capacitor. **(10 Marks)**

7 a. With a neat circuit schematic, explain the working of a fulladder implemented using dynamic logic. **(07 Marks)**

b. Explain the simple delay element using clocked CMOS logic. **(07 Marks)**

c. Explain the design steps involved in analog circuit design. **(06 Marks)**

8 a. With a neat circuit schematic, explain the design of mixed signal op-amp. **(14 Marks)**

b. Explain fully differential op-amp. **(06 Marks)**

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